



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,427	07/11/2003	Colin Stephen Gormley	6834	3233

7590 02/07/2005

Attn: Matthew E. Connors
Samuels, Gauthier & Stevens, LLP
Suite 3300
225 Franklin Street
Boston, MA 02110

EXAMINER

PERKINS, PAMELA E

ART UNIT	PAPER NUMBER
----------	--------------

2822

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/617,427

Applicant(s)

GORMLEY ET AL.

Examiner

Pamela E. Perkins

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 July 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 11 July 2003. Claims 1-38 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-7, 11, 28-31 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gormley (6,818,564) in view of Peeters et al. (6,300,665).

Referring to claims 1 and 36-38, Gormley discloses a method for forming a micro-mechanical component in a semiconductor wafer where a membrane layer (3) supported on a handle layer (5) with a buried insulating layer (4) disposed between the membrane layer (3) and the handle layer (5), the micro-mechanical component (7) being formed in the membrane layer (3), and a communicating opening (10) extending through the handle layer (5) and the buried insulating layer (4) exposing the micro-mechanical component (7) (Fig. 3; col. 5, line 59 thru col. 6, line 1); forming at least one trench (8) extending through the membrane layer (3) for defining the micro-mechanical component (7) therein, each trench exposing a portion of the buried insulating layer (4) bridging the trench (8) (Fig. 2: col. 7, lines 16-24).

Gormley does not disclose applying a support layer to each bridging portion of the buried insulating layer, the support layer extending across each trench, and being applied to each bridging portion of the buried insulating layer prior to the bridging portion being exposed by the communicating opening through the handle layer for supporting the bridging portion for preventing rupturing of the buried insulating layer when the buried insulating layer is exposed by the communicating opening through the handle layer.

Peeters et al. disclose a method for forming a micro-mechanical component in a semiconductor wafer where a membrane layer (1403) supported on a handle layer (1401) with a buried insulating layer disposed between the membrane layer (1403) and the handle layer (1041) (Fig. 14b; col. 10, lines 8-21), the micro-mechanical component (405) being formed in the membrane layer (1401), and a communicating opening (1450) extending through the handle layer (1401) and the buried insulating layer exposing the micro-mechanical component (405) (Fig. 14l); forming at least one opening extending for defining the micro-mechanical component (405) therein, each opening exposing a portion of the membrane layer (1401) bridging the openings, applying a support layer (1408) to each bridging portion (Fig. 14f; col. 10, lines 21-35), the support layer (1408) extending across each opening, and being applied to each bridging portion prior to the bridging portion being exposed by the communicating opening (1450) through the handle layer (1401) for supporting the bridging portion for preventing rupturing of the buried insulating layer when the buried insulating layer is exposed by the communicating opening through the handle layer (col. 5, lines 4-17).

Since Gormley and Peeters et al. are both from the same field of endeavor, a method of forming a micro-mechanical component in a semiconductor wafer, the purpose disclosed by Peeters et al. would have been recognized in the pertinent art of Gormley. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gormley by a support layer to each bridging portion of the buried insulating layer, the support layer extending across each trench, and being applied to each bridging portion of the buried insulating layer prior to the bridging portion being exposed by the communicating opening through the handle layer as taught by Peeters et al. to tilt the micro-mechanical component on different axes (col. 5, lines 18-40).

Referring to claim 36, "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted).

A "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972); *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); *In re Fessmann*, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and

that an old or obvious product, whether claimed in "*product by process*" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear.

Referring to claim 2, Peeters et al. disclose applying the support layer (1408) by back filling the corresponding opening (Fig. 14f; col. 10, lines 33-35).

Referring to claim 3, Peeters et al. disclose applying the support layer (1409) to the surface of the micro-mechanical component (405) in a plane parallel to the plane of the exposed surface of the membrane layer (1403) for preventing bowing of the micro-mechanical component (405) when the communicating opening (1450) has been formed in the handle layer (1401), and prior to the buried insulating layer adjacent the micro-mechanical component (405) exposed by the communicating opening (1450) being removed (Fig. 14h; col. 10, lines 39-43).

Referring to claims 4-6, Peeters et al. disclose applying the support layer (1409) to the entire exposed surface of the micro-mechanical component (405) (Fig. 14h; col. 10, lines 39-43).

Referring to claim 7, Peeters et al. disclose depositing the support layer (1408) (col. 10, lines 33-35).

Referring to claim 11, Peeters et al. disclose the support layer (1408) as a photo-resist material (col. 10, lines 33-35).

Referring to claim 28, Peeters et al. disclose removing the buried insulating layer and the support layer (1408) when the communicating opening (1450) has been formed in the handle layer (1401) (Fig. 14i; col. 11, lines 2-6).

Referring to claim 29, Peeters et al disclose removing the buried insulating layer before removing the support layer (1408) (Fig. 14k; col. 10, lines 59-67).

Referring to claim 30, Peeters et al. disclose removing the support layer (1408) and the buried insulating layer simultaneously (Fig. 14l; col. 11, lines 2-6).

Referring to claim 31, Gormley discloses the micro-mechanical component (7) is a micro-mirror supported in the membrane layer (3) by a pair of tethers (8) located on opposite sides of the micro-mirror for defining a pivot access about which the micro-mirror is tiltable (col. 5, line 66 thru col. 6, line 12).

Claims 8-10, 12-27 and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gormley in view of Peeters et al. as applied to claim 1 above, and further in view of Flanders et al. (6,341,039).

Gormley in view of Peeters et al. disclose the subject matter claimed above except wherein the support layer comprises a first support layer, and a second support layer applied over the first support layer.

Flanders et al. disclose a method for forming a micro-mechanical component in a semiconductor wafer where a membrane layer (B) supported on a handle layer (A) with a buried insulating layer (X1) disposed between the membrane layer (B) and the handle layer (A), the micro-mechanical component being formed in the membrane layer (B), and a communicating opening extending through the handle layer (A) and the buried insulating layer (X1) exposing the micro-mechanical component (Fig. 4G; col. 6, lines

45-63); forming at least one trench extending through the membrane layer (B) for defining the micro-mechanical component therein (Fig. 4C: col. 6, lines 26-34).

Referring to claim 14, Flanders et al. disclose forming a support layer (C) applied over the structure (Fig. 4D; col. 6, lines 35-44).

Since Gormley and Flanders et al. are both from the same field of endeavor, a method for forming a micro-mechanical component in a semiconductor wafer, the purpose disclosed by Flanders et al. would have been recognized in the pertinent art of Gormley. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gormley by forming a support layer over the membrane layer as taught by Flanders et al. to improve performance (col. 1, lines 19-50).

Referring to claims 8, 15, 19 and 21, Flanders et al. disclose the support layer comprising oxide, silicon or polysilicon (col. 6, lines 35-38).

Referring to claims 9, 10, 17 and 18, Flanders et al. disclose the depth of the oxide support layer is in the order of 1 μm (col. 6, lines 30-32).

Referring to claims 12 and 13, Peeters et al. disclose the photoresist support layer of claim 1 wherein the photoresist support layer is of a depth of 500 nm¹ (col. 10, lines 33-35). It is noted that the specification contains no disclosure of either the critical nature of the claimed concentrations or any unexpected results arising there from. It would have been obvious to one of ordinary skill in the art to form the photoresist support layer with a depth of 5 μm since it has been held that "In such an situation, the

¹ 500 nm = 0.5 μm

Art Unit: 2822

applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.” *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) See MPEP § 2144.05.

Referring to claims 16 and 20, Peeters et al. disclose depositing the support layer (1408) (col. 10, lines 33-43).

Referring to claims 22 and 23, Flanders et al. disclose the support layer of claim 1 wherein the support layer is of a depth in the range of 15 to 25 microns (col. 6, lines 240-43). It is noted that the specification contains no disclosure of either the critical nature of the claimed concentrations or any unexpected results arising there from. It would have been obvious to one of ordinary skill in the art to form the support layer with a depth of 4 μm since it has been held that “In such an situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.” *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) See MPEP § 2144.05.

Referring to claim 24, Flanders et al. disclose the support layer (C) comprises a silicon wafer (col. 6, lines 35-44).

Referring to claims 25 and 26, Flanders et al. disclose the support layer (C) in the form of a silicon wafer, while it is acting as a support layer is of depth in the range of 15 μm to 25 μm (col. 6, lines 40-43).

Referring to claim 27, Flanders et al. disclose etching an access opening through the support layer (C) for providing access to the micro-mechanical component (Fig. 4H; col. 7, lines 4-10).

Referring to claims 32 and 33, Flanders et al. disclose the membrane layer of claim 1 wherein the membrane is of a depth in the range of 6 to 10 microns (col. 6, lines 26-30). It is noted that the specification contains no disclosure of either the critical nature of the claimed concentrations or any unexpected results arising there from. It would have been obvious to one of ordinary skill in the art to form the membrane layer with a depth of 3 μm since it has been held that "In such an situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) See MPEP § 2144.05.

Referring to claims 34 and 35, Flanders et al. disclose the buried insulating layer of claim 1 wherein the buried insulating layer is of a depth in the range of 2 to 4 microns (col. 6, lines 19-21). It is noted that the specification contains no disclosure of either the critical nature of the claimed concentrations or any unexpected results arising there from. It would have been obvious to one of ordinary skill in the art to form the buried insulating layer with a depth of 0.4 μm since it has been held that "In such an situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) See MPEP § 2144.05.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571)


Art Unit: 2822

272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP


AMIR ZARABIAN
SUPERVISOR, PATENT EXAMINER
ELECTRONIC BUSINESS CENTER